Ni is above a threshold voltage of M_N, the NMOS device of the inverter will turn on and clamp the voltage at N to a low voltage level. Under these conditions, the voltage between node N and VDD (Fig. 4), Vgs, decreases from 0 volts to a negative voltage. Whenever the value of Vgs is less than the threshold voltage of M_{ESD}, M_{ESD} will be turned-on. The threshold voltage of M_{ESD}, which is referred to as Vthp, is about -0.86 volts in the circuit shown in Fig. 4.

IN THE CLAIMS

Please amend the claims as follows.

1. (Amended) An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

a ESD pulse clamp means comprising a PMOS device for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a

second port that is connected to said second terminal of said IC, and a third port; and

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means, whereby in detecting a presence of said electrostatic pulse said ESD pulse detection means generates a voltage that triggers said ESD pulse clamp means thereby shunting said electrostatic pulse from said IC.

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10. (Amended) The circuit of claim 1, said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second port and a third port.

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20. (Amended) An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be

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caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means comprising a PMOS device for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

A5 an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component, a capacitive component, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said

NMOS device are commonly connected to said third port of said voltage inverter, said connection of bulk and drain of said PMOS device is commonly connected to said first port of said voltage inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of said voltage inverter, said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter;

said capacitive component of said ESD pulse detection means comprising a first terminal and a second terminal, said first terminal of said capacitive component being connected to said first terminal of said IC;

said resistive component of said ESD pulse detection means comprising a first terminal and a second terminal, said second terminal of said resistive component being connected to said second terminal of said IC, and said second terminal of said capacitive component and said first terminal of said resistive component being commonly connected to said third port of said voltage inverter; and

said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second port and a third port, said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said

second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said ESD pulse clamp means, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of gate said PMOS device is connected to said third port of said ESD pulse clamp means.

22. (Amended) An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means comprising a PMOS device for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component having a first and a second terminal, a capacitive component having a first and a second terminal, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said NMOS device are commonly connected to said third port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said voltage inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of said voltage inverter, said connection of source

of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter;

said capacitive component of said ESD pulse detection means comprises a PMOS device having connections of gate electrode, source, drain and bulk whereby said connections of source, drain and bulk of said PMOS device are commonly connected to said first terminal of said capacitive component, said connection of gate is connected to said second terminal of said capacitive component.

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said resistive component of said ESD pulse detection means comprising a first terminal and a second terminal, said second terminal of said resistive component being connected to said second terminal of said IC, and said second terminal of said capacitive component and said first terminal of said resistive component being commonly connected to said third port of said voltage inverter; and

said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second port and a third port, said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse